YC1089

Bluetooth 4.2 BLE

Datasheet

Yichip Microelectronics

Revision History

Version	Date	Author	Description
preliminary	2019-04-01	L.D	Initial version
V1.1	2019-04-09	L.D	Modified Pin Function Description
V1.2	2019-09-24	LY.G	Update Schematic

General Description

The YC1089 is a very low power, high performance and highly integrated Bluetooth 4.2 BLE solution, designed for operation over the 2400MHz to 2483.5Mhz ISM frequency band.

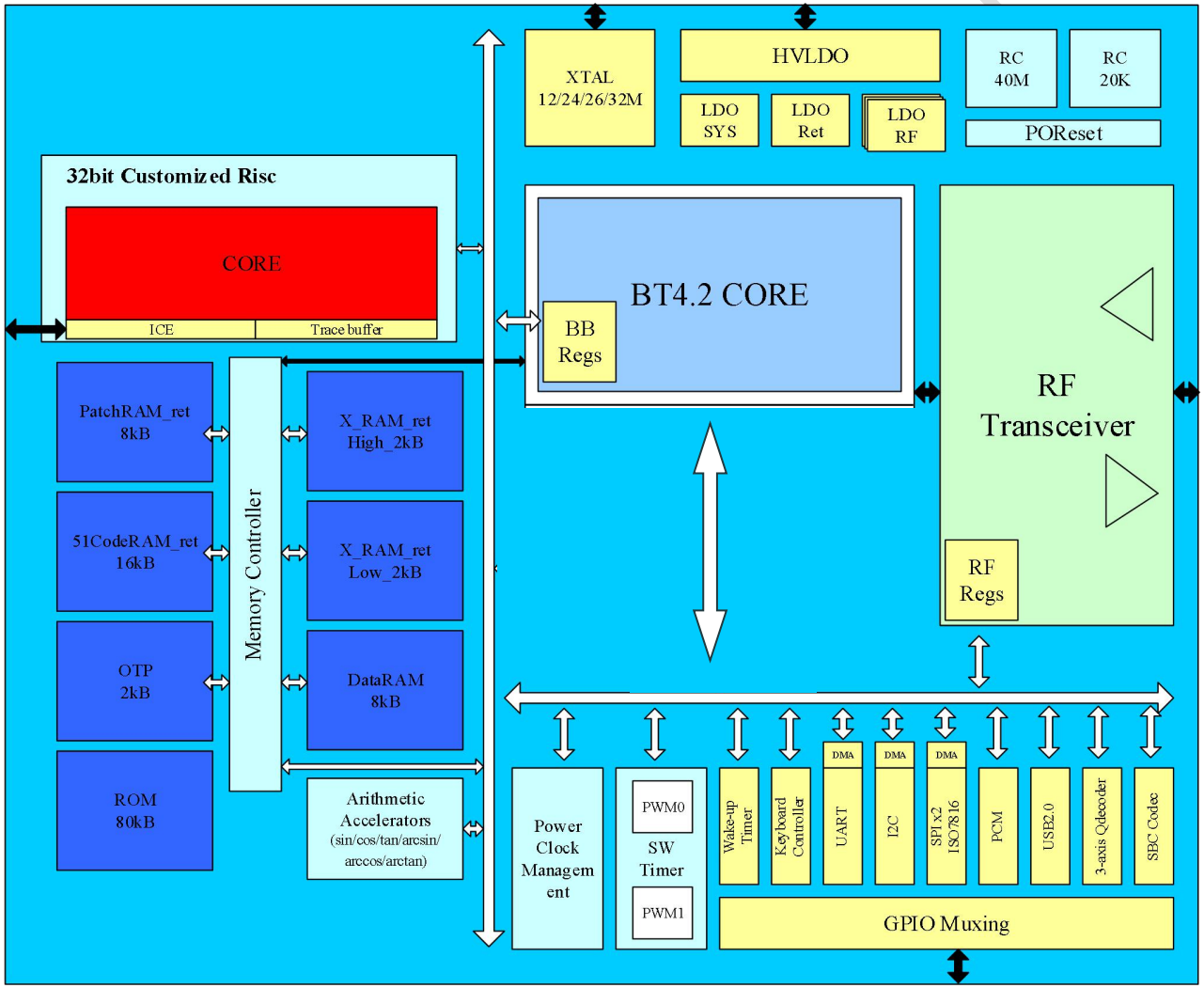
YC1089 is manufactured using advanced 55nm CMOS low leakage process, which offers highest integration, lowest power consumption, lowest leakage current and reduced BOM cost while simplifying the overall system design. Rich peripherals including an 8 channel general purpose ADC, power-on-reset (POR), Arithmetic Accelerators, 3axis Q-decoder, ISO7816, UART/SPI/I2C and up to 9 GPIOs, which further reduce overall system cost and size.

YC1089 operates with a power supply range from 1.8 to 5.5V and has very low power consumption in both Tx and Rx modes, enabling long lifetimes in battery-operated systems while maintaining excellent RF performance. The device can enter an ultra low power sleep mode in which the registers and retention memory content are retained while low power Oscillator and sleep timer is ON.

Key Features

- Bluetooth 4.2 BLE
- Very Low Power Consumption
  - 10nA shut down mode (external interrupts)
  - 900nA sleep mode (32kHz RC OSC, sleep timer and register ON)
  - 2uA retention mode (32kHz RC OSC, sleep timer, 2k retention memory and register ON)
  - Rx peak current @3V (ideal DCDC)
    - 6.75mA in BLE mode
  - Tx peak current @3V (-2dBm, ideal DCDC)
    - 16.5mA in BLE mode
  - Rx peak current w/o DCDC
    - 16mA in BLE mode
  - Tx peak current w/o DCDC @ -2dBm
    - 22mA in BLE mode
  - <25uA avg, 500ms sniff hold connection
- 2.4GHz Transceiver
  - Single-end RFIO
  - -93dBm in BLE mode
  - support 250kbps, 1Mbps data rates
  - Tx Power upto +6dBm
- Oscillators
  - 16M/24M/32M XTAL supported (default 24M)
  - 50M RC oscillator
  - Low Jitter 32K RC oscillator
- Single Core Digital Architecture
  - 32bit-Risc Core for link management
    - 80kB code ROM
    - 8kB code RAM
    - All RAMs can be set to retention mode
- Arithmetic Accelerators *[Accuracy : (sign, 15b.16b)]*
  - multi/div/sqrt
- Analog Peripherals
  - 8 channel ADC with 10 bit accuracy/3Msps
- Digital Peripherals
  - Two-wire Master (I2C compatible), upto 400kbps; UART(RTS/CTS) with HCI-H5 protocol, upto 3.25Mbps; SPI Master, upto 24Mbps
  - ISO7816
  - AES128 HW encryption
  - LED drive capability
  - PWM
  - 1 axis Q-decoder

Block Diagram



Electrical Specifications

Name	Parameter (Condition)	Min	Typ	Max	Unit	Comment
Power Supplies						
HVIN	Voltage Input, typically 1uF decouple cap	3.1	4.2	5.5	V	(1)
HVOUT	Voltage Output, typically 1uF decouple cap, maximum 50mA load capability	2.75	2.85	2.95	V	
IQ_HV	Quiescent Current of high voltage LDO		750		nA	
VIN	Voltage Input, typically 1uF decouple cap	1.5		3.6	V	
VINPA	Voltage Input, typically 5pF decouple cap	1.5		3.6	V	(2)
VIO	Voltage Input	1.7		3.6	V	(3)
DVDD	Voltage Output, typically 1uF decouple cap	1.1	1.2	1.3	V	
VDDLPM	Voltage Output, typically 100nF decouple cap	1.1	1.2	1.3	V	
Temperature						
TEMP	Temperature	-20		+85	℃	
Digital Input Pin						
VIH	High Level	VIO-0.3		VIO+0.3	V	
VIL	Low Level	VSS		VSS+0.3	V	
Digital Onput Pin						
VOH	High Level	VIO-0.3		VIO+0.3	V	(4)
VOL	Low Level	VSS		VSS+0.3	V	
Current Consumption						
IVDD	Shut down mode, can only be waked up by wake-up pin.		10		nA	
IVDD	Retention mode (LPO, no retention RAM, POR, sleep timer, I/O interrupts ON), can be waked up by sleep timer & any GPIO		0.70		uA	(5)
IVDD	Retention mode (LPO, 2kB retention RAM, POR, sleep timer, I/O interrupts ON), can be waked up by sleep timer & any GPIO		1.25		uA	
IVDD	RX mode, BLE & 2.4G mode, 100% ON (with ideal DCDC @3V)		6.75		mA	(6)
IVDD	TX mode, BLE & 2.4G mode, 100% ON (with ideal DCDC @3V)		16		mA	(7)
IVDD	Average Current, 500ms sniff, hold connection			25	uA	
Normal RF Condition						
FOP	Operating Frequency	2400		2480	MHz	
FXTAL	Crystal Frequency	12	24	32		(8)
Transmitter Characteristics						
PRF	RF output power	-20	0	6	dBm	

CD	Carrier Drift Rate		5		kHz/50us	
PRF1	Out of band emission 2 MHz (GFSK)		-40		dBm	
PRF2	Out of band emission 3 MHz (GFSK)		-48		dBm	
BW	20dB bandwidth		0.9		MHz	
EVM	Modulation Accuracy, RMS DEVM (π /4 DQPSK)		7	20	%	
	Modulation Accuracy, RMS DEVM (8PSK)		7	13	%	
	Modulation Accuracy, 99% DEVM (π /4 DQPSK)		14	30	%	
	Modulation Accuracy, 99% DEVM (8PSK)		14	20	%	
	Modulation Accuracy, Peak DEVM (π /4 DQPSK & 8PSK)		18	35	%	
	Modulation Accuracy, Peak DEVM (8PSK)		18	25	%	
PRF1	Out of band emission 2 MHz (π /4 DQPSK & 8PSK)		-30	-20		
PRF2	Out of band emission 3 MHz (π /4 DQPSK & 8PSK)		-42	-40		
Receiver Characteristics						
	BT4.0 (BLE)					
SEN	High Gain mode, Sensitivity @0.1%		-93		dBm	
SEN	Standard Gain mode, Sensitivity @0.1%		-87		dBm	
MaxIn	Maximum Input Power		0		dBm	
C/ICO	Co-channel C/I, Basic Rate, GFSK		7		dB	
C/I1ST	ACS C/I 1MHz, Basic Rate, GFSK		5.5	7	dB	
C/I2ND	ACS C/I 2MHz, Basic Rate, GFSK		-36	-34	dB	
C/I3RD	ACS C/I 3MHz, Basic Rate, GFSK		-43		dB	
C/I1STI	ACS C/I Image channel, Basic Rate, GFSK		-34		dB	
C/I2NDI	C/I 1MHz adjacent to image channel, Basic Rate, GFSK		-28		dB	

(1) HVIN & HVOUT are input & output of a high voltage LDO which is integrated in YC1089, input voltage range from 3.1~5.5V, and maximum load capability upto 50mA. Typically used in Li_BAT (3.2~4.2V) or USB_Power(4.5~5.5V) applications. If input voltage is lower than 3.6V, HVIN & HVOUT should be left unconnected and YC1089 should be powered by VIN/VINLPM/VINPA directly.

(2) If RF output power should be larger than -4dBm, VINPA should be larger than 2.5V.

(3) VIO should always be powered ON in all working cycles.

(4) Drive capability of GPIO[6:7] & GPIO[18:22] is up to 30mA, other GPIO's drive capability is 10mA

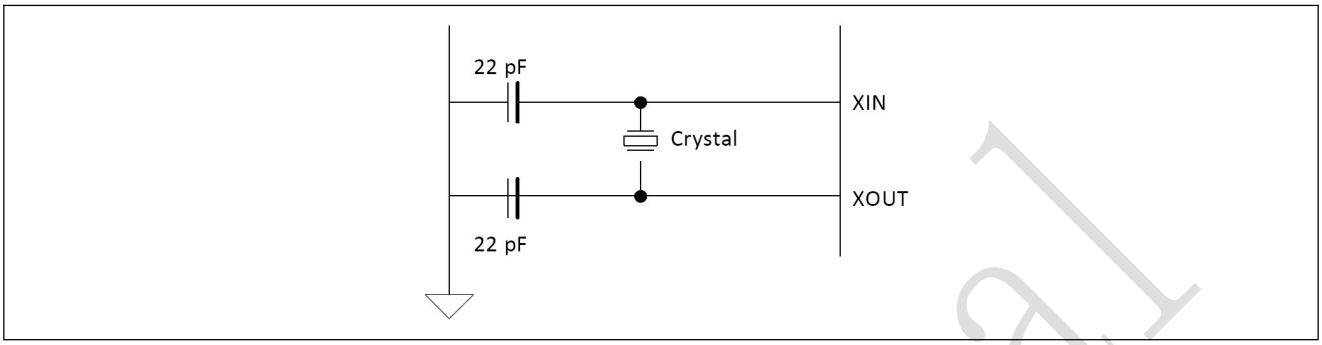
(5) By default, 2kB retention memory is ON in retention mode. Up to 4kB retentionable X_memory available at the cost of extra 600nA retention mode current. Result based on standard gain mode

(6) Result based on -2dBm Pout

(7) 12M, 16M, 24M, 26M, 32M crystal supported, 24M by default

Crystal Oscilator

The crystal oscillator requires a crystal with an accuracy of ±30 ppm as defined by the Bluetooth specification. Two external load capacitors in the range of 5 pF to 30 pF are required to work with the crystal oscillator. The selection of the load capacitors is crystal dependent. The recommended crystal specification shows below.



Recommended Oscillator Configuration — 20 pF Load Crystal

Reference Crystal Electrical Specifications

Name	Parameter (Condition)	Min	Typ	Max	Unit	Comment
Frequency			24		MHz	
Oscillation mode			Fundamental			
Frequency tolerance	@25°C		±10	±30	ppm	
Tolerance stability over temp	@0°C to +70°C		±10	±30	ppm	
Load capacitance			20		pF	
Operating temperature range		-20		+70	degree	
Drive Level			100		uW	

Power consumption

W/O DC-DC	Parameter	Average Current	Unit
Sleep	/	700	nA
Sniff	500ms interval	21.99	uA
Discoverable	ADV interval: 640ms Scan interval: 1280ms Scan window: 11.25ms	138.66	uA

With DC-DC	Parameter	Average Current	Unit
Sleep	/	700	nA
Sniff	Sniff Interval:500ms	17.92	uA
Discoverable	ADV interval: 640ms Scan interval: 1280ms Scan window: 11.25ms	89.5	uA

Bluetooth Security

1. Pairing
   - Pin Code

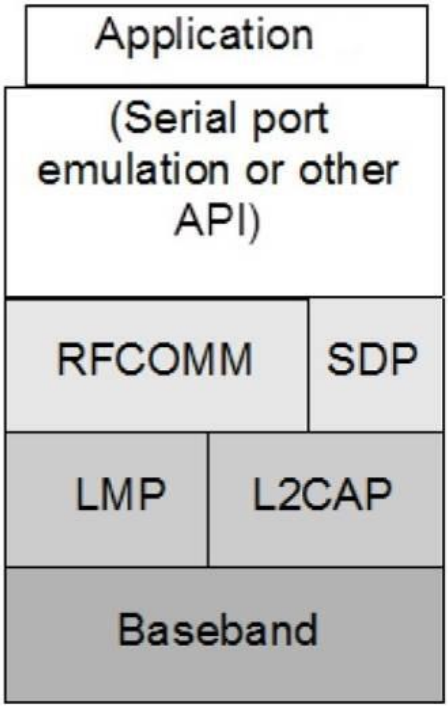
2. Security Simple Pairing
   - Just Work(No input)
   - Keyboard
   - DisplayYesNo

MFi

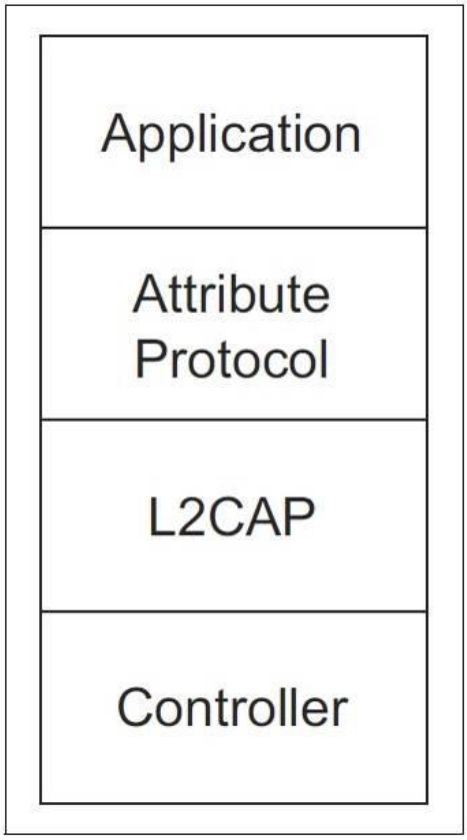
Support Apple’s MFi authentication and iAP1/iAP2 protocols.

Bluetooth Stack

1. Serial Port Profile

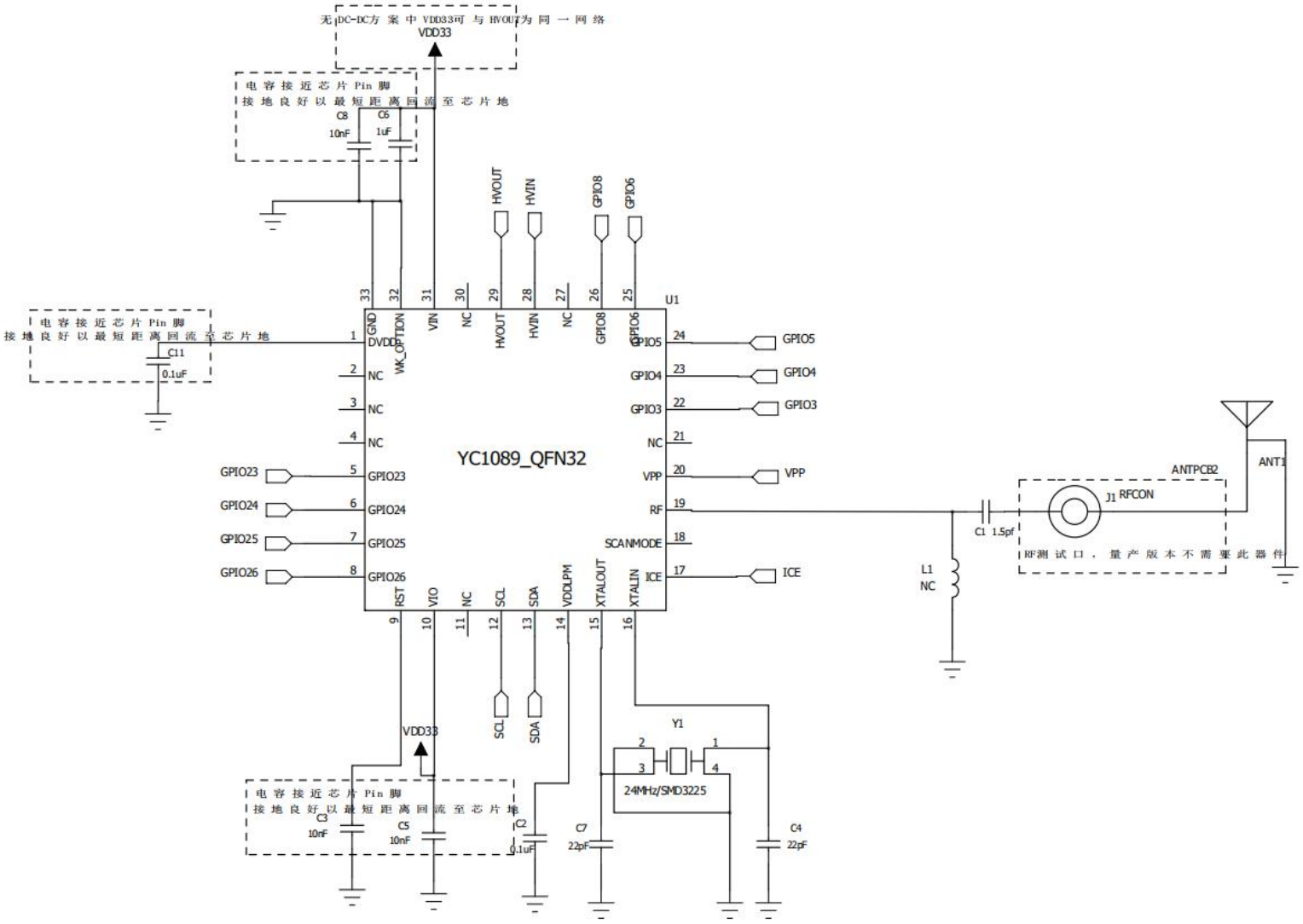


2. Generic Attribute Profile



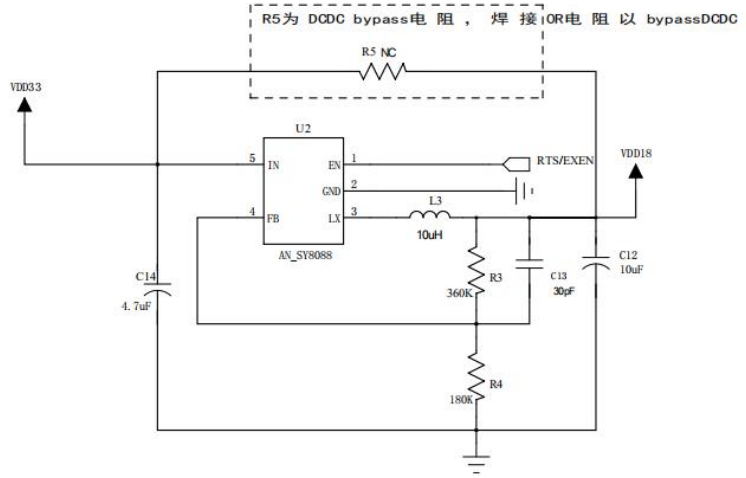
Application Schematic

1. Transparent transmission application

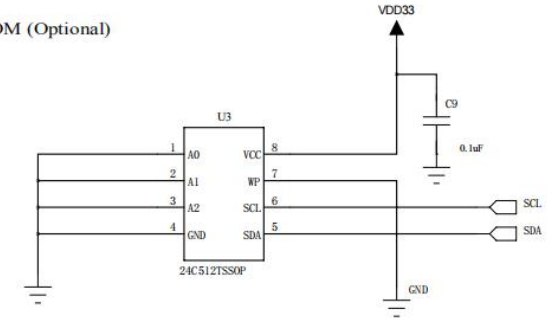


DC-DC BUCK

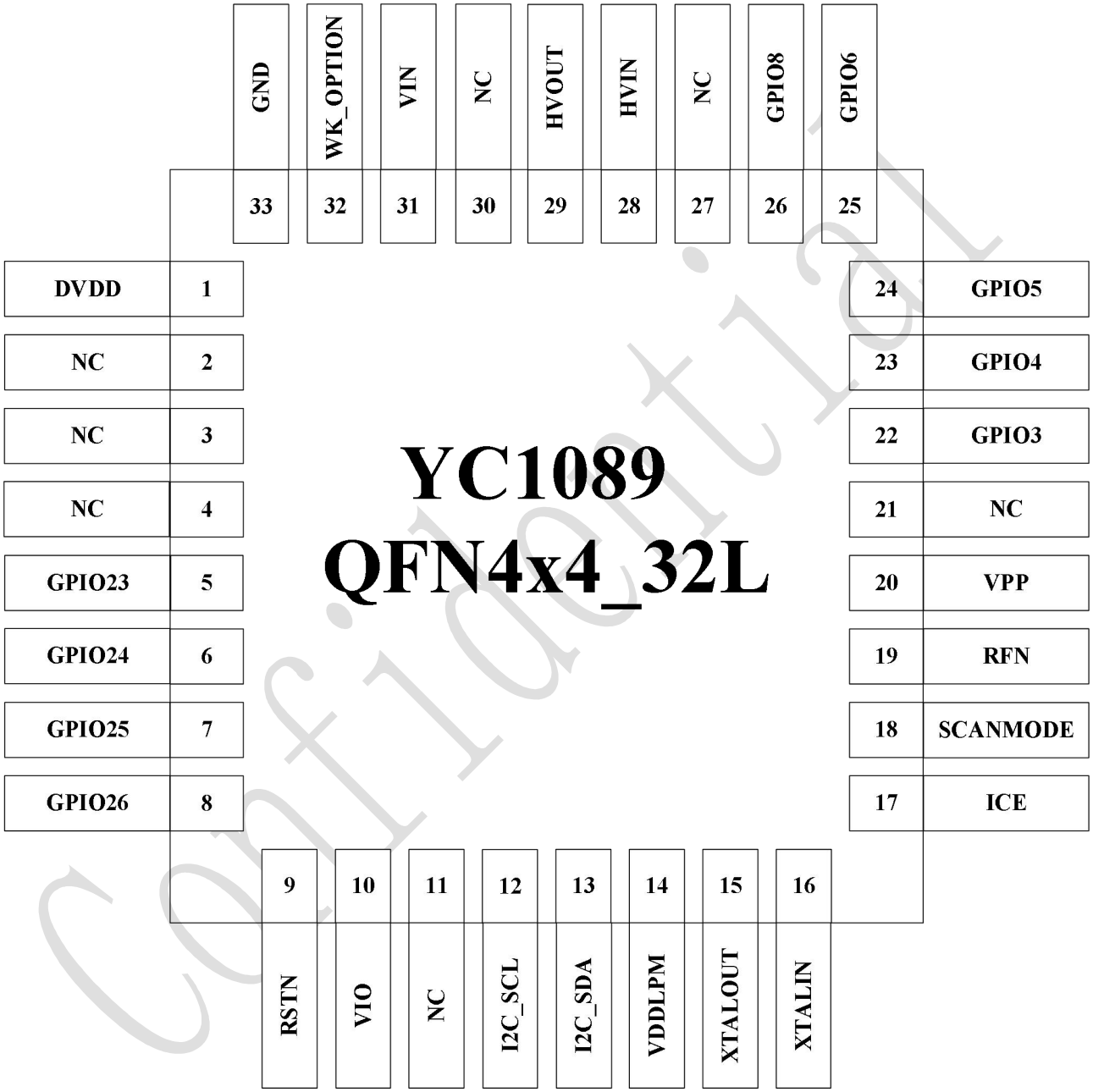
注 意 ：DC-DC为 可 选 电 路 ， 有 DC-DC时 将 VDD18与 VDD33连 成 同 一 网 络
选 用 DC-DC时 ， GPIO2选 作 EXEN功 能



EEPROM (Optional)



Package Information



4x4 32L	Pin Name	Type	Function Description
32	WK_OPTION	Power_I	Shut down mode select,active low.If not needed connect with VINPA.
1	DVDD	Power_O	internal LDO output, 1.2V. Need an external bypass cap here 1uF
2	USBDP	Dig_IO	USB port.
3	USBDN	Dig_IO	USB port.
/	GPIO17	Dig_IO	pls check "sheet: GPIO_Muxing"
/	GPIO18	Dig_IO	pls check "sheet: GPIO_Muxing"
/	GPIO19	Dig_IO	pls check "sheet: GPIO_Muxing"
/	GPIO20	Dig_IO	pls check "sheet: GPIO_Muxing"
/	GPIO21	Dig_IO	pls check "sheet: GPIO_Muxing"
/	GPIO22	Dig_IO	pls check "sheet: GPIO_Muxing"
4	GPIO23	Dig_IO	pls check "sheet: GPIO_Muxing"
5	GPIO24	Dig_IO	pls check "sheet: GPIO_Muxing"
6	GPIO25	Dig_IO	pls check "sheet: GPIO_Muxing"
7	GPIO26	Dig_IO	pls check "sheet: GPIO_Muxing"
8	GPIO27	Dig_IO	pls check "sheet: GPIO_Muxing"
9	RSTN	Dig_I	Gloable reset, active low. OR gated with internal POR. NC if not needed.
10	VIO	Power_I	I/O Power, 1.8~3.6V， 100nF//10pF bypass cap
11	GPIO28	Dig_IO	pls check "sheet: GPIO_Muxing"
/	GPIO29	Dig_IO	pls check "sheet: GPIO_Muxing"
/	GPIO30	Dig_IO	pls check "sheet: GPIO_Muxing"
/	GPIO31	Dig_IO	pls check "sheet: GPIO_Muxing"
12	I2C_SCL	Dig_IO	Internal pull up 1Kohm to VIO and no need external pull up resistor.
13	I2C_SDA	Dig_IO	Internal pull up 1Kohm to VIO and no need external pull up resistor.
14	VDDLPM	Power_O	internal LDO output, 1.2V. Need an external bypass cap here 100nF
15	XTALOUT	Ana_O	XTAL port
16	XTALIN	Ana_I	XTAL port, or external CLK in
17	ICE	Dig_IO	debug port, Tx & Rx
18	SCANMODE	Dig_I	SCAN Test enable pin
19	RFN	RF Port	ANT port
/	RFP	RF Port	ANT port
/	GPIO0	Dig_IO	pls check "sheet: GPIO_Muxing"
/	GPIO1	Dig_IO	pls check "sheet: GPIO_Muxing"
20	VPP	Power_I	OTP Program Power, 6.5V
21	GPIO2	Dig_IO	pls check "sheet: GPIO_Muxing"
22	GPIO3	Dig_IO	pls check "sheet: GPIO_Muxing"
23	GPIO4	Dig_IO	pls check "sheet: GPIO_Muxing"
24	GPIO5	Dig_IO	pls check "sheet: GPIO_Muxing"

25	GPIO6	Dig_IO	pls check "sheet: GPIO_Muxing"
26	GPIO7	Dig_IO	pls check "sheet: GPIO_Muxing"
27	GPIO8	Dig_IO	pls check "sheet: GPIO_Muxing"
/	GPIO9	Dig_IO	pls check "sheet: GPIO_Muxing"
/	GPIO10	Dig_IO	pls check "sheet: GPIO_Muxing"
/	GPIO11	Dig_IO	pls check "sheet: GPIO_Muxing"
/	GPIO12	Dig_IO	pls check "sheet: GPIO_Muxing"
/	GPIO13	Dig_IO	pls check "sheet: GPIO_Muxing"
/	GPIO14	Dig_IO	pls check "sheet: GPIO_Muxing"
/	GPIO15	Dig_IO	pls check "sheet: GPIO_Muxing"
/	GPIO16	Dig_IO	pls check "sheet: GPIO_Muxing"
28	HVIN	Power_I	HV LDO input, 3~5.5V, 4.7uF bypass cap
29	HVOUT	Power_O	HV LDO output, 2.85V. Bypass cap need here, 1uF
30	NC	NC	NC
31	VINPA	Power_I	Tx_PA's power supply, 1.8~3.6V,100nF//5pF bypass cap

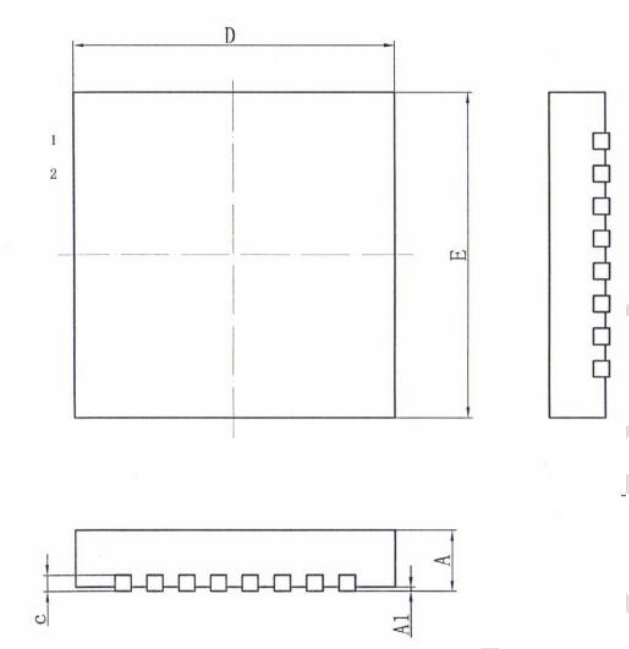
Note: Most GPIOs are by default configured to input status after power-on reset, except for GPIO2 & GPIO24/25/26 which are in output status. If a GPIO is not used as well as it is not configured to output, it can be connected to GND. But GPIO2 & GPIO24/25/26 MUST NOT be connect to GND at any time.

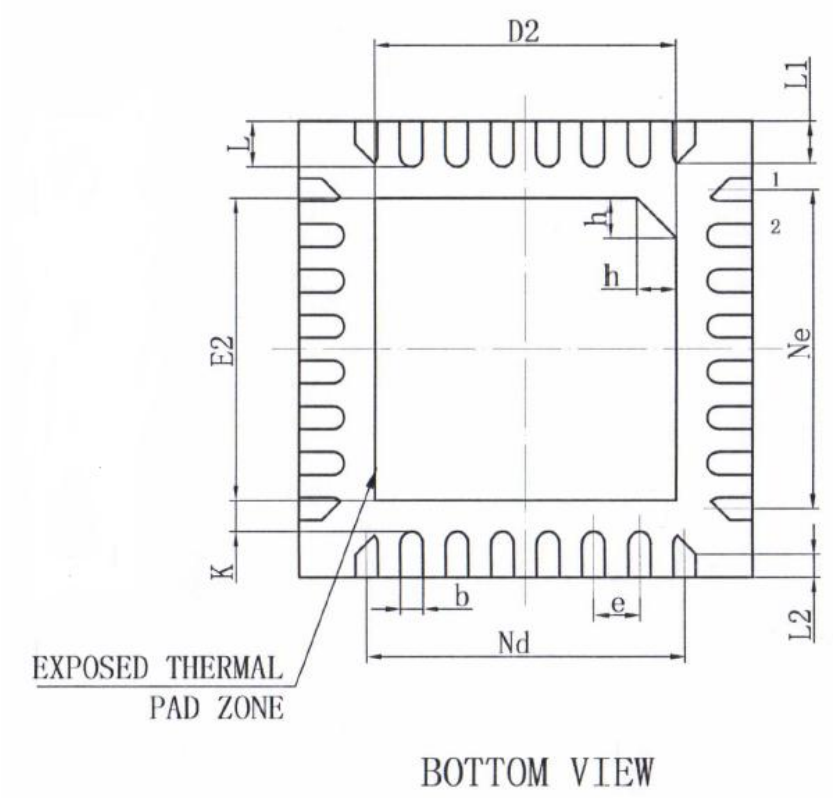
GPIO Muxing Table

GPIOs	Function1	Function2	Function-Ana
GPIO[0]			
GPIO[1]			
GPIO[2]	UARTRTS	EXEN	
GPIO[3]	UARTCTS	PWM OUT4	adc_channel1
GPIO[4]	PWM OUT0		adc_channel2
GPIO[5]	PWM OUT1		adc_channel3
GPIO[6]	UARTTX		adc_channel4
GPIO[7]	UARTRX		adc_channel5
GPIO[8]	PWM OUT5		wakeup
GPIO[9]	SPIMISO-B		
GPIO[10]	SPICS-B		
GPIO[11]	SPICLK-B		
GPIO[12]	SPIMOSI-B		
GPIO[18]			CMP-
GPIO[19]			CMP+
GPIO[20]	PWM OUT0		
GPIO[21]	PWM OUT1		
GPIO[22]	PWM OUT2		
GPIO[23]	SPIMISO		adc_channel6
GPIO[24]	SPICS		adc_channel7
GPIO[25]	SPICLK	TWSCLK	adc_channel8
GPIO[26]	SPIMOSI	TWSDAT	
GPIO[27]	PWM OUT2	ZA	
GPIO[28]	PWM OUT3	ZB	
GPIO[29]			
GPIO[30]	SCL	TWSCLK	
GPIO[31]	SDA	TWSDAT	
GPIO[32]	ICE		

Note: Drive capability of GPIO[3:5] & GPIO[27:29] is up to 100mA,GPIO8 internal pulldown also can drive 100mA, other GPIO's drive capability is 10mA.

Package Physical Dimension (QFN4x4_32L)





SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.60	2.65	2.70
e	0.40BSC		
Nd	2.80BSC		
E	3.90	4.00	4.10
E2	2.60	2.65	2.70
Ne	2.80BSC		
K	0.20	–	–
L	0.35	0.40	0.45
L1	0.30	0.35	0.40
L2	0.15	0.20	0.25
h	0.30	0.35	0.40
L/F载体尺寸 (Mil)	112*112		